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EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,149	MOSHAYEDI, MARK	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☒ Claim(s) *36-38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

1. Claims 1-39 are represented for examination.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

3. The drawings filed on 12/20/2001 have been approved by the Examiner.

Oath/Declaration

4. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Information Disclosure Statement

5. The information disclosure statement (IDS) submitted on 03/19/2002. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

6. Claims 36-38 are objected to because of the following informalities:

In claims 36-38, line 1, "The method of claim 35" should be changed to –The early failure detection system of claim 35 --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-5 and 8-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Morishita et al.,U.S. Patent 6,446,223 B1.

Regarding claims 1 and 35, Morishita teaches that an early failure detection method for a flash memory system wherein the flash memory system designates a quantity of storage locations as spares locations (Fig.12, spare blocks), the spares locations being assigned for use as alternate storage locations in the event that defects occur (col.3, lines 18-27), the early failure detection system comprising:

evaluating the quantity of spares locations available (Fig.15, the remaining spare block count number of blocks including those in disagreement) for assignment as alternate storage locations to determine if a threshold value (Fig.12 or 15, remaining block count threshold value 2552) has been reached (Fig.15, step S416); and

in the event that the quantity of spares locations reaches the threshold limit, taking a preemptive action (Fig.15, step 418 to step 411) to avert impending failure of the flash memory system (col.1, lines 42-46).

Regarding claim 2, Morishita teaches that a method of determining the usability of a solid-state storage device, wherein the solid-state storage device comprises spare storage locations for use in the event a defect occurs in other storage locations (col.3, lines 18-27), the method comprising predicting the usability of the solid-state storage device based on the quantity of unused spare storage locations (Fig.15, step S416, the remaining spare block count number of blocks including those in disagreement can predict the usability of the storage device).

Regarding claim 3, Morishita teaches that further comprising assigning a quantity of storage locations within a solid-state storage device to serve as spare storage locations in the event defects occur in the storage locations (Fig.12, spare blocks are set in advance).

Regarding claim 4, Morishita teaches that wherein the act of predicting the usability of the solid-state storage device comprises determining whether the quantity of unused spare storage locations is less than a predetermined threshold amount (Fig.15, step S416).

Regarding claim 5, Morishita teaches that wherein the act of predicting comprises comparing the amount of unused spare storage locations to an original amount of spare storage locations (Fig.12, lines 30-35, spare block 3313 contains a remaining spare block bit map 33131 indicate status of the remaining spare blocks).

Regarding claim 8, Morishita teaches that the act of predicting calculates a currently available amount of spare storage locations as a percentage of an initially available amount of spare storage locations (Fig.12, lines 30-35, spare block 3313 contains a remaining spare block bit map 33131 indicate status of the remaining spare blocks).

Regarding claim 9, Morishita teaches that a method of monitoring the life expectancy of a flash memory device, wherein the solid-state storage device comprises spare storage locations for use in the event a defect occurs in other storage locations (col.3, lines 18-27), the method comprising:

comparing the number of available spare locations (Fig.15, the remaining spare block count number of blocks including those in disagreement) with a predetermined

threshold (Fig.12 or 15, remaining block count threshold value 2552) (Fig.15, step S416); and

performing an action (Fig.15, step 418 to step 411) when the quantity of unused spare storage locations falls below the predetermined threshold, so as to avoid the consequences of a potential failure of the flash memory (col.1, lines 42-46).

Regarding claim 10, Morishita teaches that further comprising assigning a quantity of storage locations within a flash memory device to serve as spare storage locations wherein the spare storage locations are used when defects occur in the flash memory device (Fig.12, spare blocks are set in advance within a medium 331 and the storage 3 is a flash memory as taught in col.1, lines 42-46).

Regarding claim 11, Morishita teaches that the predetermined threshold is stored in a controller in the flash memory device (the remaining spare block count threshold value 2552 is stored in 255 of cache memory 25b of the storage controller 2b as shown in Fig.11).

Regarding claim 12, Morishita teaches that the predetermined threshold is stored in a memory array (cache memory 25b as shown in Fig.11) associated with the flash memory device (Fig.11, storage 3).

Regarding claim 13, Morishita teaches that the predetermined threshold is stored in a host system (Fig.11, host system includes a host computer, a storage controller and a storage) that stores data in the flash memory device.

Regarding claim 14, Morishita teaches that the predetermined threshold is calculated as a percentage of an initial number of spare storage locations available within the flash memory device (col.5, lines 45-50).

Regarding claim 15, Morishita teaches that the predetermined threshold is calculated as a percentage of an average number of spare storage locations typically available within a flash memory device similar in memory capacity to the flash memory device (col.5, lines 45-50).

Regarding claim 16, Morishita teaches that a solid-state storage device comprising:

a plurality of storage locations (Fig.12); a plurality of spare storage locations (Fig.12, spare blocks) wherein the spare storage locations are used when defects occur in the storage locations (col.3, lines 18-27); and processor circuitry configured to predict the usability of the solid-state storage device based on the quantity of unused spare storage locations (Fig.15, step S416, the remaining spare block count number of blocks including those in disagreement can predict the usability of the storage device).

Regarding claim 17, Morishita teaches that the processor circuitry is further configured to send a notification regarding the usability of the solid-state storage device (it is taught as the remaining spare block count threshold value 2552 determine when to start the spare medium copy process).

Regarding claim 18, Morishita teaches that the processor circuitry is further configured to display the quantity of unused spare storage locations (Fig.15, step S416, remaining spare block count number of blocks).

Regarding claim 19, Morishita teaches that the processor circuitry is further configured to copy data from some storage locations to other storage locations (Fig.15, it is taught as copy process).

Regarding claim 20, Morishita teaches that the processor circuitry is further configured to automatically enable the addition of supplemental storage locations for use by the solid-state storage device (col.2, lines 57-63).

Regarding claim 21, Morishita teaches that the processor circuitry is further configured to enable a manual addition of supplemental storage locations for use by the solid-state storage device (col.1, lines 49-51).

Regarding claim 22, Morishita teaches that a flash memory device comprising:

a plurality of storage locations (Fig.12, blocks);

a plurality of spare storage locations (Fig.12, spare blocks);

a predetermined threshold value (Fig.13, remaining spare block count threshold value 2552); and

processor circuitry configured to compare the number of available spare storage locations (Fig.15, step S416, remaining spare block count number of blocks) with the predetermined threshold and wherein the processor circuitry is further configured to perform an action (Fig.15, step 418 to step 411) when the quantity of unused spare storage locations falls below the predetermined threshold (Fig.15, S416), so as to avoid the consequences of a potential failure of the flash memory (col.1, lines 42-46).

Regarding claim 23, Morishita teaches that the flash memory device is a flash memory card (col.1, lines 42-47).

Regarding claim 24, Morishita teaches that the flash memory device is a flash memory chip (col.1, lines 42-47).

Regarding claim 25, Morishita teaches that the flash memory device is an array of flash memory cards (Fig.11 and 12).

Regarding claim 26, Morishita teaches that storage locations can be dynamically allocated as spare storage locations (col.2, lines 57-63).

Regarding claim 27, Morishita teaches that the action performed by the processor circuitry allows for the use of other unused spare storage locations accessible by the flash memory device to serve as supplemental spare storage locations (col.2, lines 57-63).

Regarding claim 28, Morishita teaches that a method of determining the usability of a solid-state storage device, the method comprising:

assigning a quantity of storage locations within a solid-state storage device to serve as spare storage locations (Fig.12, spare blocks) wherein such spare storage locations are used when defects occur in the storage locations (col.3, lines 18-27);

monitoring the number of available spare storage locations (Fig.15, the remaining spare block count number of blocks including those in disagreement); and performing an action (Fig.15, step 418 to step 411) when the quantity of unused spare storage locations falls below a desired amount (Fig.15, step S416), so as to avoid the consequences of a potential failure of the solid-state storage device (col.1, lines 42-46).

Regarding claim 29, Morishita teaches that monitoring the number of available spare storage locations (remaining spare block bit map 33131) takes place within the memory device (medium 331 of storage 3).

Regarding claim 30, Morishita teaches that monitoring the number of available spare storage locations takes place within a host system (Fig.11, host system includes a host computer, a storage controller and a storage) that uses the memory device to store data.

Regarding claim 31, Morishita teaches that monitoring the number of available spare storage locations takes place within the controller of the memory device (storage controller 2b).

Regarding claim 32, Morishita teaches that monitoring the number of available spare storage locations takes place within a peripheral controller (Fig.11, transporter 32).

Regarding claim 33, Morishita teaches that monitoring the number of available spare storage locations takes place within a bus controller (Fig.11, bus 27).

Regarding claim 34, Morishita teaches that monitoring the number of available spare storage locations takes place within any processor configured to monitor the memory device (Fig.11, 26b).

Regarding claim 36, Morishita teaches that evaluating the quantity of spares locations available for assignment is carried out by referring to a counter that is incremented each time a new spares location is used (Fig.4, step S406 and col.5, lines 40-46).

Regarding claim 37, Morishita teaches that evaluating the quantity of spares locations available for assignment is carried out by counting all available spares locations at predetermined time intervals (col.7, lines 37-43 and lines 56-64).

Regarding claim 38, Morishita teaches that evaluating the quantity of spares Locations available for assignment is carried out upon request by a host system (it is taught as the spare block copy process 265 is carried out upon request by a host system for writing operation).

Regarding claim 39, Morishita teaches that system for determining the usability of a solid-state storage device, wherein the solid-state storage device comprises spare storage locations for use in the event a defect occurs in other storage locations (col.3, lines 18-27), the system comprising:

means for monitoring the number of available spare storage locations (Fig.15, the remaining spare block count number of blocks including those in disagreement); and

means for performing an action (Fig.15, step 418 to step 411) when the quantity of unused spare storage locations falls below a desired amount (Fig.15, step S416), so as to avoid the consequences of a potential failure of the solid-state storage device (col.1, lines 42-46).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita et al., U.S. Patent 6446223 B1, as applied to claim 2 above and further in view of Arakawa., U.S. Patent 5751947.

Regarding claim 6, while Morishita teaches the act of predicting the usability of the solid-state storage device, Morishita does not teach monitoring the frequency of defects occurring. However, Arakawa teaches monitoring the frequency of defects occurring (col.5, lines 10-11). As taught by Arakawa, monitoring the frequency of defects occurring allows a warning message or an warning signal output to the host system, therefore, the data or command within the computer system can be efficiently performed (col.3, lines 60-62 and col.12, lines 24-25) and reliability related to data maintenance can be improved (col.3, lines 50-52 and col.11, lines 64-65). Accordingly,

it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Arakawa in the system of Morishita and monitor the frequency of defects occurring for the advantage stated by Arakawa (i.e. efficient data performed and data reliability).

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita et al., U.S. Patent 6446223 B1, as applied to claim 2 above, and further in view of Secrest., U.S. Patent 5541846.

Regarding claim 7, while Morishita teaches the act of predicting the usability of the solid-state storage device, Morishita does not teach monitoring the rate of change in the frequency of defects occurring. However, Secrest teaches monitoring the rate of change in the frequency of defects occurring (col.4, lines 46-48). As taught by Secrest, monitoring the frequency of defects occurring allows the system maintaining detailed defect records and enables the source of defects to be traced accurately (col.2, lines 30-32). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Arakawa in the system of Morishita and monitor the rate of change in the frequency of defects occurring for the advantage stated by Secrest.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kawashita., US patent 5283790

Chan et al., US patent 6480982 B1

Gaudet et al., US patent 5418767

Jenett., US patent 5867641

Jeddeloh., US patent 5974564

13. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

14. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-5:30 (first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7238 for regular communications and 703-746-7239 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song
Patent Examiner
August 11, 2003

Mano Padmanabhan
Supervisory Patent Examiner
Technology Center 2100